LISTING OF THE CLAIMS

1-3. (Canceled)

4. (Original) An integrated circuit memory device comprising:

a substrate assembly, said substrate assembly including a plurality of memory arrays, said memory arrays each including a plurality of memory blocks; and

first, second, and third layers of metalization, wherein one of said layers includes at least one I/O line that is continuous within said one layer over a span of two or more memory blocks.

5. (Original) A device, as in claim 4, wherein a memory array includes at least four memory blocks, and wherein said at least one I/O line is continuous within said one layer over a span of said at least four memory blocks.

6. (Original) A device, as in claim 4, wherein a memory array includes at least eight memory blocks, and wherein said at least one I/O line is continuous within said one layer over a span of said at least eight memory blocks.

7. (Original) An integrated circuit memory device comprising:

a substrate assembly including a memory array;

said memory array including a plurality of memory blocks, at least eight of said memory blocks being arranged in spaced relation to one another in a first direction relative to said substrate assembly;

a sense amplifier stripe having a longitudinal axis oriented substantially parallel to said first direction;

first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly; and

an I/O trace disposed among said traces of one of said layers having a longitudinal axis oriented substantially parallel to said first direction.

8. (Original) A device as in claim 7 wherein said I/O trace spans at least four of said eight memory blocks.

9. (Original) A device as in claim 7 wherein said I/O trace spans at least eight of said memory blocks.

10 -14. (Canceled)

15. (Original) An integrated circuit memory device comprising:

a substrate assembly;

a layer of metallic traces including a local phase line trace;

a pair of wordline driver circuits, each of said circuits including one transistor of a pair of transistors formed within a common active region of said substrate assembly, said transistors sharing a common drain, said drain having a single connection to said local phase line trace.

16. (Original) An integrated circuit memory device comprising:

a substrate assembly;

at least first, second, and third layers of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

a global bleeder circuit disposed within said substrate assembly and adapted to supply a standby voltage; and

a sense amplifier circuit disposed within said substrate assembly;

a global bleeder trace, at least a portion of which is disposed among said traces of said third layer of traces, operatively connected to both said bleeder circuit and said sense amplifier, and adapted to communicate said standby voltage from said bleeder circuit to said sense amplifier.

17-24. (Canceled)

25. (Original) An integrated circuit memory device comprising:

two adjacent wordline driver circuits;

an active area having first and second transistors formed therein;

a portion of said active area including a doped region common to said two transistors;

one of said transistors being operatively connected to said first wordline driver circuit and the other of said transistors being operatively connected to said second wordline driver circuit.

26. (Original) A device as in claim 25 further comprising a local phase line including a point of connection operatively connected to said doped region.

27. (Original) An integrated circuit memory device comprising:

a substrate assembly;

a layer of metalization over a substrate, said layer including at least one global bleeder line;

a bleeder device disposed within said substrate having an output operatively connected to said bleeder line; and

a plurality of sense amplifiers disposed within said substrate each amplifier of said plurality being operatively connected to said bleeder line.

28. (Original) A device as in claim 27 further comprising:

a plurality of additional layers of metal traces;

said plurality of layers disposed between said global bleeder line and said substrate assembly.

29. (Original) A device as in claim 27 further comprising:

a memory array block;

said block disposed within said substrate assembly;

one of said plurality of sense amplifiers being disposed on one side of said block, and another of said plurality of sense amplifiers being disposed on a second opposite side of said block.

30. (Original) An integrated circuit memory device comprising:

a substrate assembly;

first and second memory arrays formed in said substrate assembly, said arrays disposed in spaced relation to one another and defining a throat therebetween;

a row decoder disposed in said substrate assembly within said throat;

a layer of metallic traces disposed in substantially parallel spaced relation over said substrate assembly; and

a global wordline trace disposed within said layer;

said global wordline trace being operatively connected to both said row driver and at least one of said arrays.

31. (Original) A device as in claim 30 further comprising:

at least one data read line and one data write line;

said lines being disposed adjacent said throat and within said layer of metallic traces.

32. (Canceled)

33. (Original) A method of operating an integrated circuit memory device, said method comprising:

providing a layer of metalized traces including a plurality of I/O traces;

including within said layer a plurality of non-I/O traces, and disposing at least one non-I/O trace between two I/O traces;

introducing a first plurality of I/O signals, each exhibiting a transient portion and a non-transient portion, onto said plurality of I/O traces respectively;

introducing a second plurality of non-I/O signals, each exhibiting a transient portion and a non-transient portion, onto said plurality of non-I/O traces respectively, and applying said signals such that said I/O signal transient portions occur only during non-transient portions of said non-I/O signals.

34. (Canceled)

35. (Original) A method of operating an integrated circuit memory device comprising:

providing an integrated circuit including a substrate assembly and a layer of metallic traces disposed in substantially parallel spaced relation over said substrate assembly;

providing among said third layer of metallic traces a first plurality of I/O traces interspersed with a second plurality of non-I/O traces such that at least one non-I/O trace is disposed between any two of said I/O traces;

during a first time period, introducing a first plurality of electrical signals each including a transient portion followed by a non-transient portion, one onto each of said non-I/O traces respectively, and allowing each of said first plurality of signals to reach said non-transient portion;

during a second time period, subsequent to said first time period, introducing a second plurality of electrical signals, each including a transient portion followed by a non-transient portion, one onto each of said plurality of I/O traces respectively such that said transient portion of said second electrical signal occurs exclusively during said non-transient portion of said first electrical signal.

36. (Currently amended) A method as in claim 35 further comprising providing a plurality of additional layers of metalization, wherein said plurality of I/O traces is spaced farther from said substrate than any of said additional layers.

37. (Original) A method of forming an integrated circuit memory device comprising:

forming a first layer of metallic traces over a substrate assembly which contains a plurality of sense amplifier portions;

forming a second layer of metallic traces over and insulated from said first layer of traces;

said second layer of traces including a first plurality of column select trace portions positioned over said sense amplifier portions;

forming a third layer of metallic traces over and insulated from said second layer of traces;

said third layer of traces including a plurality of I/O traces disposed above and substantially orthogonal to said column select traced portions; and

forming a further plurality of column select trace portions, which are substantially orthogonal to said I/O traces.

38. (Original)A method of forming an integrated circuit memory device, said method comprising:

forming first and second adjacent wordline driver circuits, each containing respective transistors;

forming said transistors within a common active region such that both share a doped region;

forming a phase line; and

operatively connecting said phase line to said doped region.

39. (Original)A method of forming an integrated circuit memory device comprising:

forming first, second, and third layers of metallic traces disposed above a substrate in spaced proximal, intermediate, and distal relation thereto respectively;

said first layer of traces including a plurality of digit lines;

said third layer of traces including a plurality of column select lines, said column select lines being disposed substantially parallel to said digit lines; and

said second layer of traces including a further plurality of traces disposed between said digit lines and said column select lines and substantially orthogonal to both said digit lines and said column select lines.

40. (Original) A method of forming an integrated circuit memory device comprising:

providing a substrate assembly;

providing a layer of metal traces disposed in substantially parallel spaced relation above said substrate assembly, said layer including a local phase trace;

providing an active region within said substrate assembly;

disposing first and second transistor gate assemblies in spaced relation above said active region, thereby defining first and second transistors; and

operatively connecting said local phase trace to said active region between said first and second gate assemblies, thereby operatively connecting said local phase trace to both said first and second transistors.

41. (Original) A method as in claim 40 further comprising:
providing a plurality of additional layers of metal traces; said plurality of layers disposed between said local phase trace and said substrate assembly.

42. (Original) A method of supplying a standby voltage to a sense amplifier of an integrated circuit memory device comprising:

providing a substrate assembly;

providing a layer of metallic traces disposed in substantially parallel spaced relation above said substrate assembly;

disposing within said layer of traces a global bleeder trace;

providing within said substrate assembly a bleeder circuit, said bleeder circuit being adapted to supply a standby voltage for a sense amplifier;

providing within said substrate assembly a plurality of sense amplifiers;

operatively connecting said global bleeder trace to said bleeder circuit;

operatively connecting said global bleeder trace to each sense amplifier of said plurality of sense amplifiers; and

operating said bleeder circuit and supplying said each sense amplifier with said standby voltage.

44. (Original) A method of connecting a wordline in a memory integrated circuit comprising:

providing a substrate assembly including first and second memory arrays disposed in spaced relation to one another and defining a throat region therebetween;

providing within said throat region a row decoder circuit having a plurality of inputs and an output;

providing a plurality of address traces;

operatively connecting said plurality of address traces to said plurality of row decoder circuit inputs respectively;

providing first and second wordline driver circuits, each having an input and an output, within said first and second memory arrays respectively;

operatively connecting said output of said row decoder to said inputs of said first wordline driver circuit and to said input of said second wordline driver circuit; and

providing, within said first and second arrays respectively, first and second wordlines operatively connected to said respective outputs of said first and second wordline drivers.

45. (Canceled)

46. (New) An integrated circuit memory device comprising:

a substrate;

first and second arrays of memory cells disposed on said substrate in spaced relation to one another;

a throat region of said substrate disposed between said first and second arrays of memory cells; and

peripheral circuitry disposed within said throat region and coupled to both said first and second arrays of memory cells.

47. (New) An integrated circuit memory device as defined in claim 46 wherein said peripheral circuitry is adapted to control an operation of at least one memory cell of said first array of memory cells.

48. (New) An integrated circuit memory device as defined in claim 46 wherein said peripheral circuitry is coupled to said first and second arrays of memory cells by an LT line.

49. (New) An integrated circuit memory device as defined in claim 48,wherein said LT line comprises a Damascene process LT line.

50. (New) An integrated circuit memory device as defined in claim 48 wherein said throat region has a first longitudinal axis, and said LT line has a second longitudinal axis, said first and second longitudinal axes being disposed in substantially perpendicular relationship to one another.

51. (New) An integrated circuit memory device as defined in claim 48 wherein said LT line is disposed parallel to first and second sense amplifier stripes of said first and second memory arrays respectively.

52. (New) An integrated circuit memory device as defined in claim 46 further comprising:

a third array of memory cells disposed on said substrate in spaced relation to said first array of memory cells; and

a further throat region of said substrate disposed between said first and third arrays of memory cells, said further throat region including further peripheral circuitry.

53. (New) An integrated circuit memory device as defined in claim 46 wherein said peripheral circuitry comprises a global phase driver line.

54. (New) A control circuit for an integrated circuit of memory device comprising:

an input coupled to a source of an address selection signal;

an address decoder circuit for decoding said address selection signal; and

an output coupled to first and second memory arrays respectively, said first and second memory arrays being disposed on a semiconductor substrate and separated from one another by a throat region, said decoder circuit being disposed within said throat region.